

Application No. 09/973,019  
Reply to Office Action of June 18, 2003

**Amendments to the Specification:**

**Please replace the paragraph beginning on page 18, line 18, with the following rewritten paragraph:**

FIG. 20A is a cross sectional view showing one step, which follows the step shown in FIG. 19, of the manufacturing method of the main construction of the semiconductor device according to the second embodiment of the present invention;

FIG. 20B is a cross sectional view showing the step, which follows the step shown in FIG. 19 and corresponds to the step shown in FIG. 9B, for explaining the manufacturing method of the partial construction of the semiconductor device according to the second embodiment of the present invention;

**Please replace the paragraph beginning on page 42, line 22, with the following rewritten paragraph:**

The manufacturing method of the nonvolatile semiconductor memory device according to the second embodiment of the present invention, which is constructed as shown in FIG. 13, will now be described in detail with reference to FIGS. 14 to 20B.

**Please replace the paragraph beginning on page 46, line 10, with the following rewritten paragraph:**

In the next step, the third side wall 19 formed of a silicon oxide film on the silicon nitride film 82 is removed by etching with, for example, ammonium fluoride as shown in FIG. 20A. As a result, all the side walls of the gates of the memory cell transistor 2, the

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NMOS transistor 4 and the PMOS transistor 75 are formed of silicon nitride and have substantially the same thickness.

**Please replace the paragraph beginning on page 46, line 27, with the following rewritten paragraph:**

Incidentally, the low voltage PMOS transistor and the low voltage NMOS transistor are formed by the method similar to that employed in the first embodiment and, thus, the detail description of the manufacturing process with reference to the drawing is omitted here. Structures of the low voltage PMOS transistor and the low voltage NMOS transistor correspond to step of FIG. 20A are shown in Fig. 20B.